ABSTRACT OF THE DISCLOSURE

Provided is a manufacturing method of a semiconductor integrated circuit device having a plurality of first MISFETs in a first region and a plurality of second MISFETs in a second region, which comprises forming a first insulating film between two adjacent regions of the first MISFET forming regions in the first region and the second MISFET forming regions in the second region; forming a second insulating film over the surface of the semiconductor substrate between the first insulating films in each of the first and second regions; depositing a third insulating film over the second insulating film; forming a first conductive film over the third insulating film in the second region; forming, after removal of the third and second insulating films from the first region, a fourth insulating film over the surface of the semiconductor substrate in the first region; and forming a second conductive film over the fourth insulating film; wherein the third insulating film remains over the first insulating film in the second region. The present invention makes it possible to raise the threshold voltage of a parasitic MOS and in addition, to suppress occurrence of an NBT phenomenon.